ELECTROPHORECTIC DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] This application claims the priority of Korean Patent Application No. 2003-0025561, filed on April 22, 2003, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

(a) Field of the Invention

[0002] The present invention relates to an electrophoretic display device.

(b) Description of the Related Art

[0003] An electrophoretic display device (EPD) is one of flat panel display devices that are used for electronic books. The EPD includes two panels including field-generating electrodes and a plurality of micro-capsules interposed between the panels. Each micro-capsule includes electric ink containing a plurality of white and black pigment particles that are negatively and positively charged respectively. Upon application of an electric field in the micro-capsules, the black and white particles move in opposite directions to display images.

[0004] The electrophoretic display is described in detail in the U.S. Patent No. 6,017,584 entitled "Multi-color electrophoretic displays and materials for making the same", issued January 25, 2000 and assigned to E-ink corporation, which is hereby incorporated by reference in its entirety.

[0005] The EPD has high reflectance and contrast regardless of viewing directions and thus it is comfortable for a viewer to see a screen of the EPD as if he sees a paper. Since the micro-capsule has bistability of black and white states, it maintains the shape without a constant

supply of voltages across the micro-capsule, once set for black or white. Accordingly, the EPD requires less power consumption. In addition, the EPD does not require polarizers, alignment layers, liquid crystal, etc., that are expensive components for a liquid crystal display, which reduces the manufacturing costs.

[0006] However, since the conventional EPD does not have a black matrix for covering the areas that are not controlled by the field-generating electrodes, the light leaks between pixels and current due to the photocurrent generated by incident lights coming from outside.

SUMMARY OF THE INVENTION

[0007] The present invention provides a high quality EPD that shows reduced current leakage. In order to reduce the current leakage induced by the incident light on the semiconductor layer of the thin film transistor, the present invention provides varieties of ways blocking lights that may have reached the semiconductor layer of the thin film transistor. It may include adopting different structures of the thin film transistor or blocking the semiconductor layers with opaque layers such as Mo or Mo alloy. The present invention also provides a color EPD. The color EPD has red, green and blue micro-capsules. It may also have black, white, yellow, magenta or cyan micro-capsules.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The present invention will become more apparent by describing embodiments thereof in detail with reference to the accompanying drawings.

[0009] Fig. 1 is a schematic diagram of an EPD according to an embodiment of the present invention.

[0010] Fig. 2 illustrates a manufacturing method of the EPD shown in Fig. 1 according

to an embodiment of the present invention.

[0011] Fig. 3 is a layout view of an EPD according to an embodiment of the present invention.

[0012] Fig. 4 is a sectional view of the EPD shown in Fig. 3 taken along the line IV-IV'.

[0013] Fig. 5 is a layout view of a TFT array panel for an EPD according to an embodiment of the present invention.

[0014] Fig. 6 is a sectional view of the TFT array panel shown in Fig. 5 taken along the line VI-VI'.

[0015] Fig. 7 is a layout view of a TFT array panel for an EPD according to an embodiment of the present invention.

[0016] Fig. 8 is a sectional view of the TFT array panel shown in Fig. 7 taken along the line VIII-VIII'.

[0017] Fig. 9 is a sectional view of a TFT array panel according to another embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

[0018] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

[0019] In the drawings, the layers, films and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is

referred to as being "directly on" another element, there are no intervening elements present.

[0020] Now, EPDs and TFT array panels therefor according to embodiments of the present invention will be described with reference to the accompanying drawings.

[0021] An EPD according to an embodiment of the present invention will be described in detail with reference to Figs. 1 and 2.

[0022] Fig. 1 is a schematic diagram of an EPD according to an embodiment of the present invention and Fig. 2 illustrates a manufacturing method of the EPD shown in Fig. 1 according to an embodiment of the present invention.

[0023] Referring to Fig. 1, an EPD according to this embodiment includes a pair of field-generating electrodes E1 and E2 and a plurality of micro-capsules 20 interposed between the electrodes E1 and E2.

[0024] Each micro-capsule 20 includes electric ink 23 containing a plurality of white and black pigment particles 21 and 22. One is negatively charged and the other is positively charged.

[0025] In order to display color image, the pigment particle 21 can be red, green, blue, cyan, yellow or magenta.

[0026] When voltage are applied to the electrodes E1 and E2, the white particle 21 and the black particle 22 move in opposite directions to color the surface of the micro-capsule and an observer 300 can see a black and white image.

[0027] Referring to Fig. 2, an array of pixel electrodes (not shown) as a kind of field-generating electrodes are formed on a panel 100 called a thin film transistor (TFT) array panel including a plurality of TFTs (not shown) connected to the pixel electrodes and a plurality of signal lines (not shown) connected to the TFTs. On the contrary, a common electrode (not shown), another field-generating electrode, is formed on another panel 200 called a common

electrode panel including a flexible plastic film 210.

[0028] A plurality of micro-capsules 220 are dispersed into an adhesive 230. A front-plane lamination (FPL) including the adhesive 230 and the common electrode panel 200 is coated on a backplane, i.e., the TFT array panel 100 by using a laminator 500.

[0029] An EPD according to an embodiment of the present invention will be described in detail with reference to Figs. 3 and 4.

[0030] Fig. 3 is a layout view of an EPD according to an embodiment of the present invention, and Fig. 4 is a sectional view of the EPD shown in Fig. 3 taken along the line IV-IV'.

[0031] An EPD according to this embodiment includes a TFT array panel 100, a common electrode panel 200, a plurality of capsules 220 interposed between the panels 100 and 200, and an adhesive 230 for combining the panels 100 and 200.

[0032] Concerning the common electrode panel 200, a common electrode 240 preferably made of transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO) is formed on an insulating substrate 210 such as a flexible plastic film.

[0033] The TFT array panel 100 is now described in detail.

[0034] A plurality of gate lines 121 for transmitting gate signals are formed on an insulating substrate 110. Each gate line 121 extends substantially in a transverse direction and a plurality of portions of each gate line 121 form a plurality of gate electrodes 123. Each gate line 121 includes an end portion 125 having a larger area for contact with another layer or an external device.

[0035] The gate lines 121 are preferably made of Al and Al alloy, Ag and Ag alloy, Cu and Cu alloy, Cr, Mo, Mo alloy, Ta, or Ti. The gate lines 121 may have a multi-layered structure including at least two films having different physical characteristics, a lower film and an upper

film. The upper film is preferably made of low resistivity metal such as Al containing metal, Ag containing metal, and Cu containing metal for reducing signal delay or voltage drop in the gate lines 121. On the other hand, the lower film is preferably made of material such as Cr, Mo, Mo alloy, Ta and Ti, which has good physical, chemical, and electrical contact characteristics with other materials such as ITO and IZO. A good exemplary combination of the lower film material and the upper film material is Cr and Al-Nd alloy.

[0036] The lateral sides of the gate lines 121 are inclined relative to a surface of the substrate 110, and the inclination angle thereof ranges about 20-80 degrees.

[0037] A gate insulating layer 140 preferably made of silicon nitride (SiNx) is formed on the gate lines 121.

[0038] A plurality of semiconductor stripes 150 preferably made of hydrogenated amorphous silicon (abbreviated to "a-Si") or polysilicon are formed on the gate insulating layer 140. Each semiconductor stripe 150 extends substantially in a longitudinal direction and has a plurality of projections branched out toward the gate electrodes 123. Each semiconductor stripe 150 becomes wider near the gate lines 121 to cover large areas of the gate lines 121.

[0039] An ohmic contact layer is preferably made of silicide or n+ hydrogenated a-Si heavily doped with n type impurity, and formed on the semiconductor stripes 150. The ohmic contact layer is removed at the channel area above the gate electrode 123. This divides the ohmic contact layer into 163 and 165, arranging 163 and 165 to face each other.

[0040] The lateral sides of the semiconductor stripes 150 and the ohmic contacts 163 and 165 are inclined relative to the surface of the substrate 110, and the inclination angle preferably ranges between about 20 degrees and about 80 degrees.

[0041] A plurality of data lines 171 and a plurality of drain electrodes 175 are formed on

the ohmic contact layer 163 and 165 and the gate insulating layer 140.

[0042] The data lines 171 for transmitting data voltages extend substantially in the longitudinal direction and intersect the gate lines 121. A plurality of branches of each data line 171, which project toward the drain electrodes 175, form a plurality of source electrodes 173. The source electrode 173 and the drain electrode 175 are separated from and face each other with a gate electrode 123 therebetween. A gate electrode 123, a source electrode 173, and a drain electrode 175 along with a semiconductor layer 150 form a TFT having a channel formed between the source electrode 173 and the drain electrode 175.

[0043] The data lines 171 and the drain electrodes 175 include a film preferably made of refractory metal such as Mo, Mo alloy, Cr, Ta and Ti. They may further include an additional film located thereon and preferably made of Al containing metal. Each data line 171 includes an end portion 179 having a large area for contact with another layer or an external device.

[0044] Like the gate lines 121, the data lines 171 and the drain electrodes 175 have inclined lateral sides, and the inclination angle ranges between about 20 degrees and about 80 degrees.

[0045] The ohmic contact layers 163 and 165 are interposed only between the underlying semiconductor layer 150 and the overlying data line 171 that include the source electrode 173 and the drain electrode 175. The ohmic contact layer reduces the contact resistance between the metal layer and the semiconductor layer. The semiconductor layer 150 includes a plurality of exposed portions, which are not covered with the data lines 171 and the drain electrodes 175, such as portions located between the source electrodes 173 and the drain electrodes 175. Although the semiconductor layer 150 is narrower than the data line 171 at most places, it becomes wider near the gate lines as described above to smooth the surface profile, thereby

preventing the disconnection of the data line 171.

[0046] A passivation layer 180 is formed on the data line 171 and the drain electrode 175, and the exposed portion of the semiconductor layer 150.

[0047] The passivation layer 180 is preferably made of acrylic organic material having a good planarization property and a low resistivity or low dielectric insulating material having dielectric constant lower than 4.0 such as a-Si:C:O and a-Si:O:F formed by plasma enhanced chemical vapor deposition (PECVD).

[0048] The passivation layer 180 has a plurality of contact holes 185 and 189 exposing the drain electrode 175, and the end portion 179 of the data line 171, respectively. The passivation layer 180 and the gate insulating layer 140 have a plurality of contact holes 182 exposing the end portions 125 of the gate lines 121. When the interlayer insulating layer is provided, the contact holes 182, 185 and 189 also penetrate the interlayer insulating layer.

[0049] Sidewalls of the contact holes 182, 185 and 189 are inclined relative to bottom surfaces of the contact holes 182, 185 and 189 and it is preferable that the inclination angle of the contact holes 182, 185 and 189 ranges about 30 degrees and about 80 degrees.

[0050] An interlayer insulating layer (not shown) preferably made of silicon oxide and silicon nitride may be disposed under the passivation layer 180 to cover the exposed portion of the semiconductor layer 150.

[0051] A plurality of pixel electrodes 191 and a plurality of contact assistants 192 and 199, which are preferably made of reflective metal, are formed on the passivation layer 180. The pixel electrodes 191 are physically and electrically connected to the drain electrodes 175 through the contact holes 185 such that the pixel electrodes 191 receive the data voltages from the drain electrodes 175. The pixel electrodes 191 supplied with the data voltages generate electric fields

in cooperation with the common electrode 270 on the common electrode panel 200.

[0052] Fig. 3 shows that the pixel electrodes 191 overlap the gate lines 121 and the data lines 171 to increase aperture ratio and to minimize the uncontrolled area. The above-described thick passivation layer 180 having low dielectric constant can reduce the parasitic capacitance between the pixel electrodes 191 and the gate lines 121 and the data lines 171.

[0053] The contact assistants 192 and 199 are connected to the exposed end portions 125 of the gate lines 121 and the exposed end portions 179 of the data lines 171 through the contact holes 182 and 189, respectively. The contact assistants 192 and 199 are not required but preferred to protect the exposed portions 125 and 179 and to complement adhesion between the exposed portions 125 and 179 and the external devices.

[0054] The pixel electrodes 191 and the contact assistants 192 and 199 may be made of transparent material such as ITO or IZO.

[0055] A plurality of metal pieces (not shown) made of the same layer as the gate lines 121 and the data lines 171 may be provided near the end portions 125 and 179 of the gate lines 121 and the data lines 171, respectively. The metal pieces are exposed though a plurality of contact holes in the passivation layer 180 and the gate insulating layer 140 and connected to the respective contact assistants 192 and 199.

[0056] According to another embodiment of the present invention, a light blocking layer (not shown) preferably made of insulating material containing black pigment is formed on the TFTs. The light blocking layer blocks light incident on the portions of the semiconductor layer 150 of the TFTs to prevent current leakage. The light blocking layer may be formed of the same layer as the passivation layer 180.

[0057] A TFT array panel for an EPD according to another embodiment of the present

invention will be described in detail with reference to Figs. 5 and 6.

[0058] Fig. 5 is a layout view of a TFT array panel for an EPD according to an embodiment of the present invention, and Fig. 6 is a sectional view of the TFT array panel shown in Fig. 5 taken along the line VI-VI'.

[0059] A plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of drain electrodes 175 are formed on a substrate 110, and a plurality of semiconductor islands 150 are formed thereon. A plurality of ohmic contact islands 163 and 165 are interposed between the data lines 171 and the drain electrodes 175 and the semiconductor islands 150.

[0060] A gate insulating layer 140 is formed on the semiconductor islands 150, the data lines 171, and the drain electrodes 175, and a plurality of gate lines 121 including a plurality of upwardly projecting gate electrodes 123 are formed on the gate insulating layer 140.

[0061] A TFT including a gate electrode 123, a semiconductor island 150, and source and drain electrodes 173 and 175 that are configured as described above is called a top gate type or staggered type TFT. Since the gate electrodes 123 are disposed on the semiconductor islands 150, the light incident on the semiconductor islands 150 from the top is blocked by the gate electrodes 123. On the other hand, the TFT shown in Fig. 4 is called a bottom gate type or inversely staggered type TFT and has a gate electrode that can block the light from the bottom.

[0062] A passivation layer 180 is formed on the gate lines 121 and the gate insulating layer 140. A plurality of contact holes 185 exposing the drain electrodes 175 are provided at the passivation layer 180 and the gate insulating layer 140, and a plurality of pixel electrodes 191 connected to the drain electrodes 175 through the contact holes 185 are formed on the passivation layer 180.

[0063] A TFT array panel for an EPD according to another embodiment of the present

invention will be described in detail with reference to Figs. 7 and 8.

[0064] Fig. 7 is a layout view of a TFT array panel for an EPD according to an embodiment of the present invention, and Fig. 8 is a sectional view of the TFT array panel shown in Fig. 7 taken along the line VIII-VIII'.

[0065] A plurality of semiconductor islands 150 are formed on a substrate 110, and a plurality of ohmic contact islands 163 and 165 are formed on the semiconductor islands 150.

[0066] A gate insulating layer 140 is formed on the semiconductor islands 150 and the ohmic contacts 163 and 165, and a plurality of gate lines 121 including a plurality of upwardly projecting gate electrodes 123 are formed on the gate insulating layer 140.

[0067] An interlayer insulating layer 802 is formed on the gate lines 121 and the gate insulating layer 140 and the interlayer insulating layer 802 and the gate insulating layer 140 have a plurality of contact holes 832 and 852 exposing the ohmic contacts 163 and 165, respectively.

[0068] A plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of drain electrodes 175 are formed on the interlayer insulating layer 140. The source and the drain electrodes 173 and 175 are connected to the ohmic contacts 163 and 165 through the contact holes 832 and 852.

[0069] A TFT including a gate electrode 123, a semiconductor island 150, and source and drain electrodes 173 and 175 that are configured as described above is called a planar type TFT. Similar to the TFT shown in Figs. 5 and 6, the light incident on the semiconductor islands 150 from the top is blocked by the gate electrodes 123.

[0070] A passivation layer 180 with a plurality of contact holes 185 exposing the drain electrodes 175 is formed on the data lines 171 and the interlayer insulating layer 802. A plurality of pixel electrodes 191 are formed on the passivation layer 180 and connected to the drain

electrodes 175 through the contact holes 185.

[0071] A TFT array panel for an EPD according to another embodiment of the present invention will be described in detail with reference to Figs. 3 and 9.

[0072] Fig. 9 is a sectional view of a TFT array panel according to another embodiment of the present invention.

[0073] As shown in Fig. 9, a layered structure of the TFT array panel 100 according to this embodiment is almost the same as that shown in Figs. 3 and 4. That is, a plurality of gate lines 121 including a plurality of gate electrodes 123 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 150, and a plurality of ohmic contact stripes 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of drain electrodes 175 are formed on the ohmic contacts 163 and 165, and a passivation layer 180 is formed thereon. A plurality of contact holes 185 are provided at the passivation layer 180 and the gate insulating layer 140, and a plurality of pixel electrodes 191 are formed on the passivation layer 180.

[0074] Unlike the TFT array panel shown in Figs. 3 and 4, the pixel electrodes 191 of the TFT array panel according to this embodiment are made of opaque conductive metal having low reflectance such as Mo or Mo alloy. In addition, the pixel electrodes 191 extend to cover portions of the semiconductor stripes 151 disposed between the source electrodes 173 and the drain electrodes 175, thereby reducing the current leakage in the TFTs.

[0075] While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present

invention as set forth in the appended claims.